

Application for United States Letters Patent

for

**METHOD OF MEASURING IMPLANT PROFILES USING
SCATTEROMETRIC TECHNIQUES**

by

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METHOD OF MEASURING IMPLANT PROFILES USING SCATTEROMETRIC TECHNIQUES

BACKGROUND OF THE INVENTION

5 1. FIELD OF THE INVENTION

This invention is generally directed to the field of semiconductor processing, and, more particularly, to a method of measuring dopant implant profiles using scatterometric techniques.

10 2. DESCRIPTION OF THE RELATED ART

There is a constant drive within the semiconductor industry to increase the operating speed of integrated circuit devices, *e.g.*, microprocessors, memory devices, and the like. This drive is fueled by consumer demands for computers and electronic devices that operate at increasingly greater speeds. This demand for increased speed has resulted in a continual reduction in the size of semiconductor devices, *e.g.*, transistors. That is, many components of a typical field effect transistor (FET), *e.g.*, channel length, junction depths, gate insulation thickness, and the like, are reduced. For example, all other things being equal, the smaller the channel length of the transistor, the faster the transistor will operate. Thus, there is a constant drive to reduce the size, or scale, of the components of a typical transistor to increase the overall speed of the transistor, as well as integrated circuit devices incorporating such transistors.

25 During the course of manufacturing integrated circuit devices, a variety of doped regions may be formed in a semiconducting substrate. Typically, these doped regions are formed by performing an ion implant process wherein a dopant material, *e.g.*, arsenic, phosphorous, boron, boron difluoride, etc., is implanted into localized areas of the substrate.

For example, for CMOS technology, various doped regions, sometimes referred to as wells, are formed in the substrate. The wells may be formed using either N-type or P-type dopant atoms. After the wells are formed, semiconductor devices, *e.g.*, transistors, may be formed in the region defined by the well. Of course, other types of doped regions may also be formed

5 in modern semiconductor manufacturing operations.

As modern device dimensions continue to shrink, the implant profiles of the various doped regions become very important. That is, as device dimensions shrink, parameters of the doped region, such as depth, width, dopant concentration profile, etc., become more important. Small variations in one or more of these parameters may adversely affect device performance. For example, if well implants in a given device are formed too shallow or not formed deep enough, the devices formed in the wells may exhibit excessive leakage currents.

Various parameters reflecting the profile of implanted regions, *e.g.*, depth, have heretofore been determined by performing a number of calculations. These calculations are typically based upon the implant energy, the type of dopant material, the implant dose and/or the angle of the implant process. Ultimately, the accuracy of these various calculations could be determined by performing destructive testing on the device after it was completed. For example, a completed device could be cross-sectioned, and the profile of the implant region of interest could be determined by observation using a tunneling electron microscope (TEM).

The aforementioned technique for determining profiles of implanted regions was problematic in that, in order to confirm any calculations of the profile, time-consuming destructive testing of at least some devices, either production or test devices, was required.

25 Moreover, such destructive testing was performed at a point so far removed in time from the

implantation process that the results were not readily available to enable, if desired, timely adjustment of the implant process performed on subsequently processed wafers and later processing (e.g., RTA, diffusion) of measured wafers. Thus, there is a need for a non-destructive testing methodology for determining at least some profile parameters of an implanted region formed in a semiconducting substrate.

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The present invention is directed to a method that may solve, or reduce, at least some of the problems described above.

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generate a profile trace for the implant regions, correlating the generated profile trace to at least one of a plurality of calculated profile traces, each of which have an associated implant region profile, and modifying, based upon the comparison of the generated profile trace and the calculated profile trace, at least one parameter of an ion implant process used to form 5 implant regions on subsequently processed substrates.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 is a cross-sectional view of a portion of a substrate having a plurality of implant regions formed therein, and a patterned layer of photoresist positioned above the substrate;

Figure 2 is a cross-sectional view of the device shown in Figure 1 after the patterned layer of photoresist has been removed;

Figure 3 is an isometric view of the structure depicted in Figure 2; and

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Figure 4 is a schematic representation of an illustrative system in which the present invention may be employed.

While the invention is susceptible to various modifications and alternative forms, 25 specific embodiments thereof have been shown by way of example in the drawings and are

herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

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DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

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The present invention will now be described with reference to the attached figures. Although the various regions and structures of a semiconductor device are depicted in the drawings as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality, these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features and doped regions depicted in the drawings may be exaggerated or reduced as compared to the size of those features or regions on fabricated devices. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention.

In general, the present invention is directed to a method of measuring implant profiles using scatterometric techniques. In some embodiments, the measured implant profiles are used to control one or more parameters of an ion implant process to be performed on subsequently processed wafers. As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of technologies, *e.g.*, NMOS, PMOS, CMOS, etc., and is readily applicable to a variety of devices, including, but not limited to, logic devices, memory devices, etc.

10 Figure 1 depicts an illustrative structure 11 that may be used in accordance with the present invention. The structure 11 is formed on part of a wafer comprised of, for example, silicon. As will become clear upon a complete reading of the present application, the structure 11 may be a test structure, or it may be part of an actual production integrated circuit device. As shown in Figure 1, a patterned layer of photoresist 12 is formed above a semiconducting substrate 10. The patterned layer of photoresist 12 has a plurality of photoresist features 14 defined therein. An ion implantation process, as indicated by arrows 16, is used to form a plurality of implant regions 18 in the areas of the substrate 10 not covered by the patterned layer of photoresist 12.

20 The patterned layer of photoresist 12 may be formed by a variety of known photolithography techniques. For example, the patterned layer of photoresist 12 may be comprised of a negative or a positive photoresist. The thickness 13 of the patterned layer of photoresist 12 may be varied as a matter of design choice. In one illustrative embodiment, the patterned layer of photoresist 12 has a thickness 13 that ranges from approximately 1.2-2.5 μm (12,000-25,000 \AA). Moreover, the features 14 in the patterned layer of photoresist 12 may 25 have a width 15 that may be varied as a matter of design choice. The ion implantation

process may be performed by a variety of tools used in modern semiconductor fabrication facilities for performing such operations. Moreover, the implant energy, the dopant material implanted, the concentration of dopant material, as well as the implant angle, may be varied in forming the implant regions 18 in the substrate 10.

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Next, as shown in Figure 2, the patterned layer of photoresist 12 is removed, or stripped, using a variety of known techniques. More particularly, as shown in Figure 2, each of the implant regions 18 has a width 17 and a depth 19 beneath the surface 21 of the substrate 10. Figure 3 is an isometric view of the substrate 10, and the implant regions 18, shown in Figure 2. As will be recognized by those skilled in the art after a complete reading of the present application, the implant regions 18 constitute a grating pattern that may be measured using scatterometric techniques. Typically, such a grating pattern will be formed in the scribe lines of a semiconducting substrate. The number of these implant regions 18 that may be formed on an actual device may vary. For example, the grating pattern may be formed in a 100 nm × 120 nm region in which approximately 300-400 implant regions 18 are formed (the length of which are parallel to the short side of the region). The implant regions 18 depicted in Figures 1-3 reflect the as-implanted location of those regions. However, as will be described further below, the present invention may also be used in cases where the implant regions 18 have been subjected to one or more diffusion and anneal processes.

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As stated previously, scatterometric techniques will be used to measure the implant profiles of the implant regions 18. As used herein, measuring the implant profile of the implant region 18 means measuring one or more characteristics of the implant region 18, *e.g.*, depth, width, dopant concentration, etc. For example, the implant profiles may reflect dopant concentration levels at various depths into a substrate. A variety of scatterometry type tools

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may be used with the present invention, *e.g.*, so-called 2θ -type systems and lens-type scatterometry tools. An illustrative scatterometry tool 24 comprised of a light source 20 and a detector 22 is schematically depicted in Figure 2. In general, the light source 20 is used to illuminate the structure 11, and the detector 22 takes optical measurements, such as intensity, of the reflected light. The scatterometry tool 24 may use white light, or some other wavelength or combination of wavelengths, depending on the specific implementation. Typically, the light source 20 will generate an incident beam that has a wide spectral composition and wherein the intensity of the reflected light changes slowly in comparison to changes in wavelength. The angle of incidence of the light may also vary, depending on the specific implementation. For example, a spectroscopic ellipsometer (single angle, many wavelengths), or a laser (single wavelength, many angles) may be used with the present invention. Additionally, the light source 20 and the detector 22 may be arranged in a concentric circle configuration, with the light source 20 illuminating the structure 11 from a perpendicular orientation, *e.g.*, a reflectometer. The intensity of the reflected light may be measured as s- and p- polarization over either multiple angles or at multiple wavelengths.

In general, the scatterometry tool 24 (see Figure 4) includes optical hardware, such as an ellipsometer or reflectometer, and a data processing unit loaded with a scatterometry software application for processing data collected by the optical hardware. For example, the optical hardware may include a Model OP5230 or OP5240 with a spectroscopic ellipsometer offered by Thermawave, Inc. of Fremont, California. The data processing unit may comprise a profile application server manufactured by Timbre Technologies, a fully owned subsidiary of Tokyo Electron America, Inc. of Austin, Texas and distributed by Thermawave, Inc.

Through use of scatterometry, a characteristic signature or profile trace, associated with a particular implant profile or characteristic of an implant profile, may be calculated (using Maxwell's equations and rigorous coupled wave analysis (RCWA)) for a vast variety, if not all, possible combinations of implant profiles readily anticipated by the design process.

5 The correlation between the scatterometry profile trace and the actual implant region profile may be based on a variety of characteristics or factors, including, but not limited to, the width 17 and the depth 19 of the implant regions 18, the concentration of the dopant material, and the dopant concentration profile. Variations in one or more of the characteristics will cause a significant change in the diffraction characteristics of the incident light from the light source 10. Thus, using scatterometric techniques, a unique profile trace may be established for each unique combination of implant profile characteristics, *e.g.*, depth and width. A library of profile traces corresponding to each unique combination of implant profile characteristics may be generated and stored in a library. Scatterometry libraries are commercially available from Timbre Technologies, Inc. Although not necessary, if desired, the library of calculated profile traces may be confirmed by various destructive metrology tests, where a scatterometry profile trace is measured and the actual profile of the features is subsequently measured using a cross sectional tunneling electron microscope metrology technique. Obviously, the number of combinations used to create the library may vary as a matter of design choice. Moreover, the greater the number of combinations, the greater will be the library containing the 15 appropriate signature profiles of the implant regions.

For example, in one embodiment, the width 17 of the implant regions 18 may vary between 0.25 and 1.25 μm , at an incremental value of, for example, 0.1 μm . The depth of the implant regions 18 may also vary between 0.1-0.5 μm , at an incremental value of .02 μm .

Thus, considering only these two parameters, 200 possible combinations of implant region profiles are readily anticipated by the design process.

Figure 4 depicts an illustrative system 50 that may be employed with the present invention. As shown therein, the system 50 is comprised of a scatterometry tool 24, a controller 40, and an ion implant tool 35. The scatterometry tool 24 generates a profile trace of the implanted regions 18 formed on wafers 37 that have been processed through the implant tool 35. Thereafter, in one embodiment of the present invention, the generated profile trace is compared to a preselected target profile trace. The preselected profile trace corresponds to a desired characteristic of the implant regions 18, *e.g.*, implant profiles of a certain desired depth. A determination is then made, by either the controller 40 or the scatterometry tool 35, if there is a deviation between the generated (or measured) profile trace and the target profile trace. If so, the controller 40 may then change one or more parameters of the operating recipe of the implant tool 35, such that implanted regions 18 formed in the subsequently processed wafers 39 are closer to the target profile. For example, one or more parameters of the implant process, *e.g.*, implant angle, implant energy, dopant material, and/or dopant concentration, to be performed on the subsequently processed wafers 39 may be adjusted to achieve the desired implant profile.

In another embodiment, the present invention may be employed to compare a measurement or generated trace profile to a library of such profiles, each of which corresponds to a particular implant profile. That is, in this embodiment, the method comprises generating additional profile traces for implant regions having different implant profiles, and establishing a library comprised of a plurality of the profile traces, wherein each of the plurality of traces is correlated to a particular implant profile.

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The scatterometry tool 24 is used to generate a profile trace for a given structure 11 with implant regions 18 formed thereon. The scatterometry tool 24 may sample one or more structures 11 in a given wafer in a lot or even generate a profile trace for each structure 11 in the lot, depending on the specific implementation. Moreover, the profile traces from a sample of the structures 11 may be averaged or otherwise statistically analyzed. A controller, either in the scatterometry tool 24 or elsewhere in the manufacturing plant, *e.g.*, controller 40, then compares the profile trace (*i.e.*, individual or averaged) generated by the scatterometry tool 24 to a library of calculated profile traces with known implant region profiles to correlate or match the generated or measured profile trace to a trace from the library having a known implant region profile. Based upon these comparisons, the controller 40, if needed, may adjust one or more parameters of an ion implant process to be performed on subsequently processed wafers 39 in the implant tool 35.

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As discussed previously, the implant regions 18 depicted in Figures 1-3 are depicted in their as-implanted positions, *i.e.*, prior to any anneal operations being performed on the structure 11. As will be understood by those skilled in the art, during such anneal processes, the implanted dopant atoms will migrate from their original implanted position, typically in an isotropic fashion, such that the regions 18 will spread out, both laterally and vertically downward, to some degree. As will be clear to those skilled in the art upon a complete reading of the present application, the present invention may be used to measure implant profiles either before or after such anneal processes are performed. Moreover, if desired, pre-anneal scatterometry measurements of the profiles of the implant regions 18 may be correlated to post-anneal profiles of the implant regions 18.

Based on the determined implant region profile, control equations may be employed to adjust the operating recipe of the ion implant tool 35 to account for deviations between the measured implant profile and the target implant profile. The control equations may be developed empirically using commonly known linear or non-linear techniques. The controller 40 may automatically control the operating recipes of the implant tool 35 used to form implant regions 18 on subsequently processed wafers 37. Through use of the present invention, the deviations between the profiles of implant regions formed on subsequently processed wafers and a target implant profile may be reduced.

10 In the illustrated embodiment, the controller 40 is a computer programmed with software to implement the functions described herein. Moreover, the functions described for the controller 40 may be performed by one or more controllers spread through the system. For example, the controller 40 may be a fab level controller that is used to control processing operations throughout all or a portion of a semiconductor manufacturing facility. Alternatively, the controller 40 may be a lower level computer that controls only portions or cells of the manufacturing facility. Moreover, the controller 40 may be a stand-alone device, or it may reside on the implant tool 35. However, as will be appreciated by those of ordinary skill in the art, a hardware controller (not shown) designed to implement the particular functions may also be used.

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Portions of the invention and corresponding detailed description are presented in terms of software, or algorithms and symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the ones by which those of ordinary skill in the art effectively convey the substance of their work to others of ordinary skill in the art. An algorithm, as the term is used here, and as it is used generally, is

conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of optical, electrical, or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

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It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise, or as is apparent from the discussion, terms such as "processing" or "computing" or "calculating" or "determining" or "displaying" or the like, refer to the actions and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical, electronic quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

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An exemplary software system capable of being adapted to perform the functions of the controller 40, as described, is the Catalyst system offered by KLA Tencor, Inc. The Catalyst system uses Semiconductor Equipment and Materials International (SEMI) Computer Integrated Manufacturing (CIM) Framework compliant system technologies, and is based on the Advanced Process Control (APC) Framework. CIM (SEMI E81-0699 - Provisional Specification for CIM Framework Domain Architecture) and APC (SEMI E93-0999 - Provisional Specification for CIM Framework Advanced Process Control Component) specifications are publicly available from SEMI.

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The present invention is directed to several inventive methods. In one embodiment, the method comprises providing a semiconducting substrate, forming a first plurality of implant regions in the substrate, and illuminating the first plurality of implant regions with a light source in a scatterometry tool, the scatterometry tool generating a trace profile corresponding to an implant profile of the illuminated implant regions. In another embodiment, the method comprises measuring profiles of implant regions formed in a semiconducting substrate, comprising forming a plurality of implant regions in a semiconducting substrate, illuminating the plurality of implant regions, measuring light reflected off the substrate to generate a profile trace for the implant regions, comparing the generated profile trace to a target profile trace, and modifying, based upon a deviation between the generated profile trace and the target profile trace, at least one parameter of an ion implant process used to form implant regions on subsequently processed substrates. In yet another embodiment, the method comprises measuring profiles of implant regions formed in a semiconducting substrate by forming a plurality of implant regions in a semiconducting substrate, illuminating the plurality of implant regions, measuring light reflected off the substrate to generate a profile trace for the implant regions, comparing or correlating the generated profile trace to a calculated profile trace in a library, wherein each of the profile traces in the library have an associated implant region profile, and modifying, based upon the comparison between the generated profile trace and the calculated profile trace from the library, at least one parameter of an ion implant process used to form implant regions on subsequently processed substrates.

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By adjusting one or more parameters of the implant tool 35 used to form the implant regions 18 on the wafer, as described above, the resultant implant profiles can be adjusted to reduce the overall profile variations for wafers manufactured in a given manufacturing line.

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Reduced variation equates directly to reduced process cost, increased device performance, and increased profitability.

The particular embodiments disclosed above are illustrative only, as the invention
5 may be modified and practiced in different but equivalent manners apparent to those skilled
in the art having the benefit of the teachings herein. For example, the process steps set forth
above may be performed in a different order. Furthermore, no limitations are intended to the
details of construction or design herein shown, other than as described in the claims below. It
is therefore evident that the particular embodiments disclosed above may be altered or modi-
fied and all such variations are considered within the scope and spirit of the invention.
10 Accordingly, the protection sought herein is as set forth in the claims below.